APOLLO: Automatic Partition-based Operator Fusion through Layer by Layer Optimization

Presenter: Bojian Zheng

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`presenting on behalf of`

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Outline

1. Introduction
2. Partition Phase
3. Fusion Phase
4. Putting It All Together
5. Results
6. Conclusion

Fusion in Deep Learning Compilers

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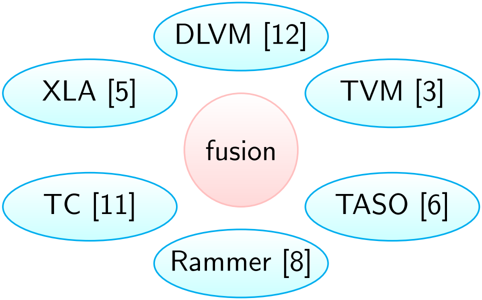

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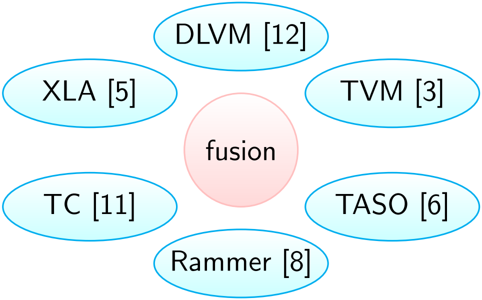
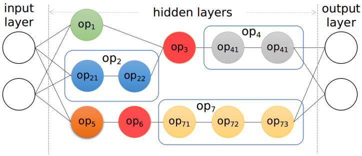


- While extensively investigated, fusion in these deep learning compilers can be inspected in different ways.

Limitations of Prior Fusion Compilers



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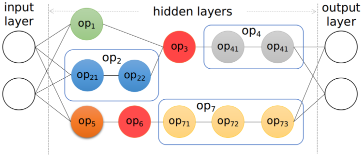

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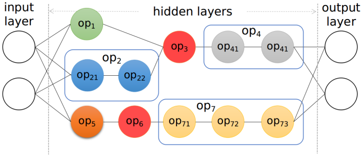

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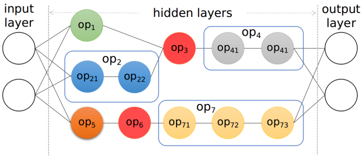

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- Tensor compilers including TVM [3], TC [11] and Tiramisu [2] execute a routine transformation orchestration (first node grouping and next loop fusion), subject to the scalability issue [15, 9] caused by the constraints from the upstream graph engine.
- More recent works [6, 8, 17] investigated horizontal fusion between independent operators, e.g., (op_1 and op_2), but training workloads and dedicated chips were rarely considered.

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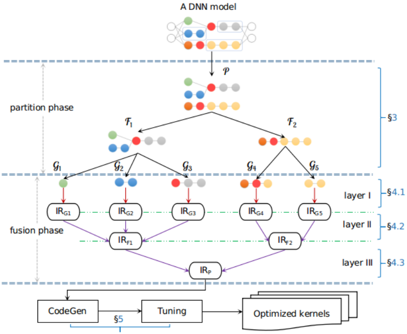

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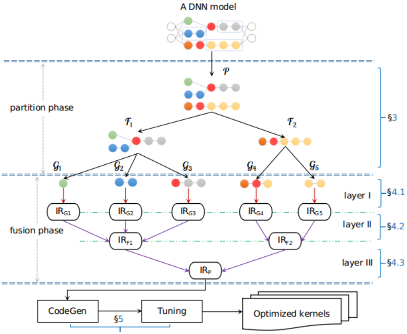

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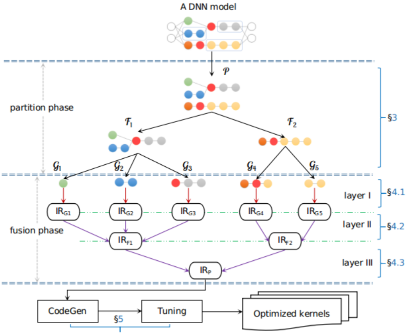

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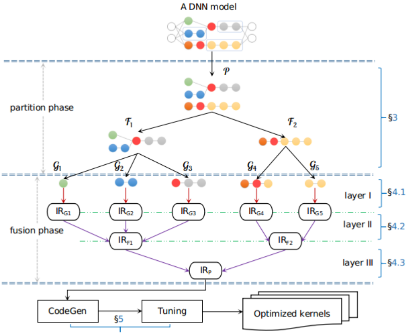

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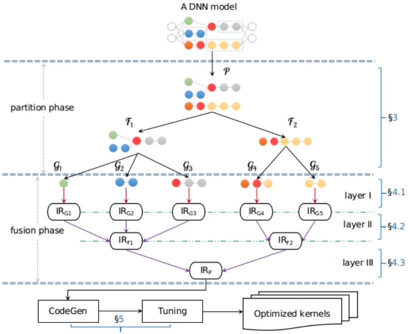

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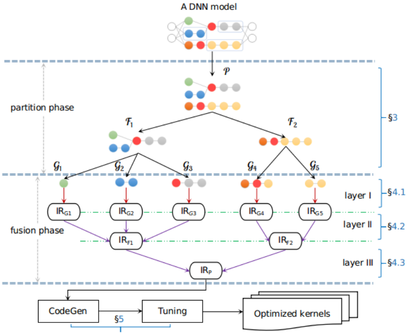

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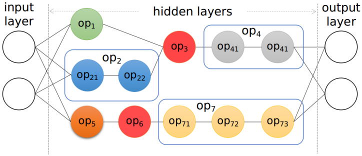
  - addresses the scalability issue of existing polyhedral compilers [16, 11];
  - goes beyond the recent works [8, 17] by enabling memory and parallelism stitching for training workloads on a dedicated accelerator.

Graph Simplification and Extracting Sub-graph Cluster $\mathcal{P}$



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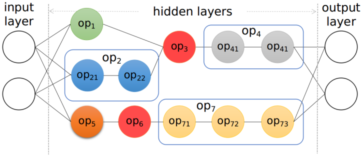

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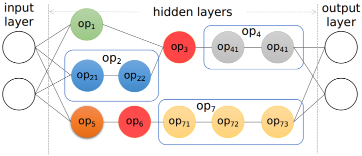

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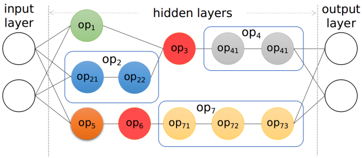

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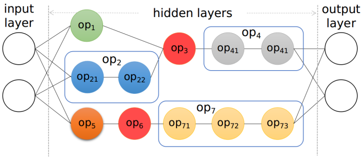

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  - user-defined and/or extraordinary operators with complex computational logic, e.g., `all-reduce` used in training speech recognition.
  - control flow operators like TensorFlow's `RefSwitch`.

Opening Compound Operators within each Sub-graph $\mathcal{F}_x$

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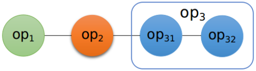

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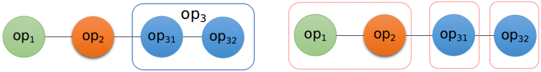

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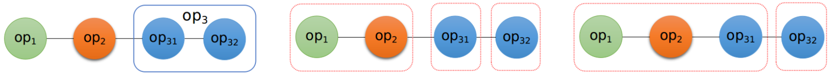

Merging Primitive Operators within each Micro-graph $\mathcal{G}_y$

- A micro-graph $\mathcal{G}_y$ is built by merging primitive operators using rules.

Rules	$\mathcal{G}_p$	$\mathcal{G}_c$	$\mathcal{G}_a$
1	element-wise	element-wise	element-wise
2	broadcast	element-wise	broadcast
3	broadcast	broadcast	broadcast
4	element-wise	reduction	reduction
5	broadcast	reduction	reduction
6-transpose	element-wise/broadcast	transpose	transpose
6-matmul	matmul	element-wise	matmul
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- In particular, the definition classifies reshaping operations, (batched) matrix multiplication and convolution as opaque operators.
- These rules do not need to cover all composition patterns of operators, since some pair of operators should not be fused.

Polyhedral Loop Fusion and its Scalability within a $\mathcal{G}_y$

- A $\mathcal{G}_y$ is converted into a sequence of loop nests and used to produce a single kernel through our prior polyhedral loop optimizer AKG [16].

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for i in [0,M)
  for j in [0,N)
    a(i,j)=a(i,j)+bias; //$S_1$
for i in [0,M/2)
  for j in [0,N/2)
    pool(i,j)=max(a(2i,2j),
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- We design and implement a framework called PANAMERA [14] to optimize a reduction not fused with its follow-up elementwise operators.

Memory Stitching between multiple $\mathcal{G}_y$'s

- Micro-graphs often end with reductions. We define complementary rules to exploit the stitching possibilities between them.

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- We rely on PANAMERA [14] to convert all reductions into three canonical forms *all*-reduce, *x*-reduce and *y*-reduce.

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for i in [0,M) and j in [0,N) and k in [0,P) and l in [0,Q)
  a(i,j,k,l) = a(i,j,k,l) + bias
for i in [0,M) and j in [0,N) and k in [0,P) and l in [0,Q)
  b(i,k) += a(i,j,k,l)
```

```
for x in [0,M*P) and y in [0,N*Q)
  a(x/P,y/Q,x%P,y%Q) = a(x/P,y/Q,x%P,y%Q) + bias
for x in [0,M*P) and y in [0,N*Q)
  b(x/P,x%P) += a(x/P,y/Q,x%P,y%Q)
```

```
for x in [0,M*P) and y in [0,N*Q){
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```

Memory Stitching between multiple $\mathcal{G}_y$'s

- Micro-graphs often end with reductions. We define complementary rules to exploit the stitching possibilities between them.

Rules	$\mathcal{G}_p$	$\mathcal{G}_c$	$\mathcal{G}_a$
7	reduction	element-wise/broadcast	reduction
8	reduction	reduction	reduction

- When performing memory stitching between $\mathcal{G}_y$'s, the complexity of an ending reduction can complicate Layer II.
- We rely on PANAMERA [14] to convert all reductions into three canonical forms *all*-reduce, *x*-reduce and *y*-reduce.

```
for i in [0,M) and j in [0,N) and k in [0,P) and l in [0,Q)
  a(i,j,k,l) = a(i,j,k,l) + bias
for i in [0,M) and j in [0,N) and k in [0,P) and l in [0,Q)
  b(i,k) += a(i,j,k,l)
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```
for x in [0,M*P) and y in [0,N*Q)
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```
for x in [0,M*P) and y in [0,N*Q){
  a(x/P,y/Q,x%P,y%Q) = ...
  b(x/P,x%P) += ...
}
```

- Canonicalizing reductions guarantees the matching between the loop dimensions of two $\mathcal{G}_y$'s that are to be stitched in faster memory.

Parallelism Stitching independent $\mathcal{G}_y$'s or $\mathcal{F}_x$'s

- Layer I & II did not consider the parallelism between $\mathcal{G}_y$'s or $\mathcal{F}_x$'s.

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$$gain = \sum_{op=m}^{k} cost_{op} - \max_{m \le op \le k}(cost_{op})$$

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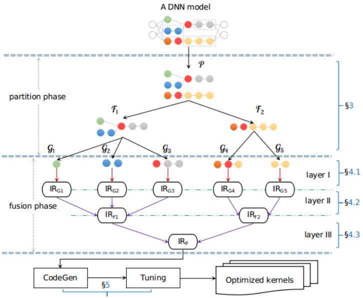
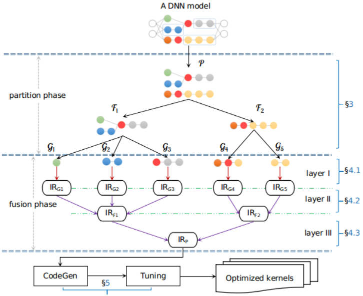
  used to determine the number of stitched operators.
- A compute-intensive operator is excluded in such a traverse, since its huge amount of data usually consumes up the hardware resources.



- To make APOLLO applicable to both training and inference workloads, APOLLO is also complemented through the following steps.

Putting It All Together



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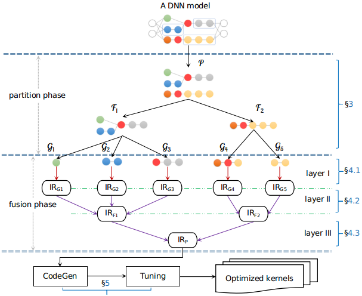

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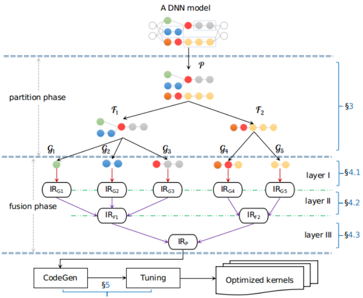

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- **Code generation** supports both GPUs and Huawei Ascend 910 chips [7].

Results on Single GPU

- Experiments are conducted using five training workloads.
- Generated CUDA code on GPUs is executed using CUDA Toolkit 10.1 with -O3 enabled.
- Generated CCE code on Ascend 910 is executed using the later's native compiler.
- The geometric mean of 10 executions is reported.
- Case study on sub-graphs, results of inference workloads and compilation overhead are reported in the paper.

Results on Single GPU

BT: BERT; TR: Transformer; WD: Wide&Deep; YO: Yolo-v3; FM: DeepFM; b.s.: batch sizes; TF: TensorFlow; MS: MindSpore; imp.: improvements

models	b.s.	TF	XLA/TF	MS	APOLLO/MS	imp.
BT-base	32	167	**105%**	135	**252%**	**39%**
	64	200.8	**129%**	183.6	**212%**	**23%**
TR	8	6750	**16%**	5122	**84%**	**20%**
	16	9500	**11%**	10868	**59%**	**64%**
WD	16000	1133696	**15%**	762086	**123%**	**48%**
	32000	1470221	**5%**	836820	**121%**	**20%**
YO	4	33.11	**15%**	39.48	**46%**	**51%**
	8	56.00	**12%**	75.01	**10%**	**31%**
FM	8192	26117	**-1%**	479744	**151%**	-
	16384	30279	**-2%**	543024	**167%**	-

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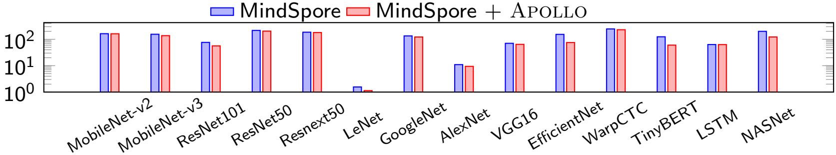

Execution times of MindSpore's model zoo (y axis: log scaled time in ms; lower is better). On average, APOLLO improves MindSpore by 29.6%.

Results on Multiple GPUs

BT: BERT; WD: Wide&Deep; FM: DeepFM; batch sizes in parenthesis; TF: TensorFlow; MS: MindSpore; imp.: improvements

models	GPUs	TF	XLA/TF	MS	APOLLO/MS	*imp.*
BT-base(32)	8	1244.9	**96%**	944.4	**247%**	**34%**
BT-base(64)	8	1555.4	**117%**	1333.1	**222%**	**27%**
BT-large(4)	4	66.94	**33%**	37.62	**133%**	**-2%**
WD(16000)	8	8086178	**1%**	4964319	**87%**	**13%**
FM(16384)	4	31767	**-7%**	2117685	**130%**	-

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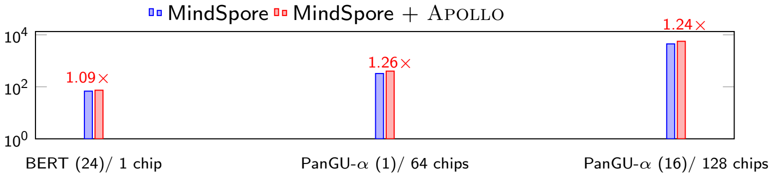
- The throughput of MindSpore falls behind, sometimes significantly, than those of TensorFlow and XLA, but it outperforms the latter two by 1.96× and 1.18×, respectively.

Results on Ascend 910 chips



Throughput of BERT and PanGu-α [13] (examples/s) on Ascend. Batch sizes are in parentheses. Higher is better.

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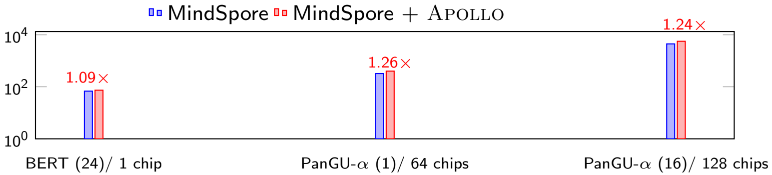

Throughput of BERT and PanGu-α [13] (examples/s) on Ascend. Batch sizes are in parentheses. Higher is better.

- APOLLO brings about a mean improvement of 19.7% over MindSpore when targeting Ascend 910 chips.

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- APOLLO addresses the scalability issue of fusion by allowing reverse feedback from the operator-level optimizer, achieving a fully automatic fusion framework;
- APOLLO enhances the performance of deep learning workloads by modeling both data locality and parallelism, producing more efficient code than the state of the art;
- APOLLO exhibits reasonable JIT compilation overhead, demonstrating its effectiveness using rather difficult real-life training workloads.

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Scan the QR code to obtain the paper/code repository/artifact.